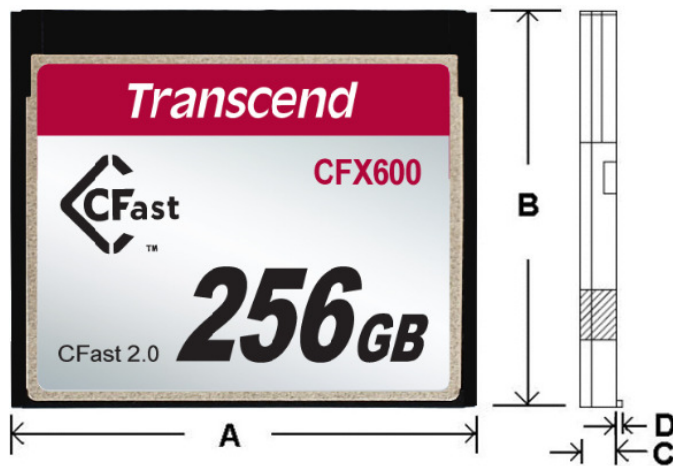# CFX600 –

CFast 2.0 Card

Transcend CFX600 is designed to satisfy high performance requirements using a SATA 6Gb/s interface. As a removable device, it is easier to plug in and remove from space-limited applications, such as thin-clients or industrial PCs. Complaint with CFast 2.0 standard, CFX600 is your best choice as an embedded SATA storage solution.

Features

- RoHS compliant
- CFast Specification Version 2.0 Compliant
- Power Supply: 3.3V±5%
- Operating Temperature: -5ºC to 70ºC
- Storage Temperature: -40ºC to 85ºC
- Humidity (non condensation): 0% to 95%
- Built-in 66bit per 1KByte ECC (Error Correction Code) functionality ensures high reliability of data transfer.
- Global wear-leveling algorithm eliminates excessive write operation and extends product life.
- Support S.M.A.R.T (Self-defined)
- Support Security Command
- Support Device Sleep
- Fully compatible with devices and OS that support the SATA 6Gb/s standard
- Durability of Connector: 10,000 times

Placement

Dimensions

Side	Millimeters	Inches
A	42.8+/-0.1	1.685+/-0.004
B	36.4+/-0.15	1.433+/-0.006
C	3.5+/-0.1	0.1378+/-0.004
D	0.6+/-0.07	0.0236+/-0.003

Specifications

Physical Specification			
Form Factor	CFast 2.0		
Storage Capacities	16GB to 256GB		
Dimensions	**Length**	42.8 ± 0.1 mm	1.685+/-0.004 inch
	Width	36.4 ± 0.15 mm	1.433+/-0.006 inch
	Height	3.5 ± 0.1 mm	0.1378+/-0.004 inch
Input Voltage	3.3V ± 5%		
Weight	10.3g		
Connector	7 + 17 pin female connector		

Environmental Specifications		
Operating Temperature	-5ºC to 70ºC	
Storage Temperature	-40ºC to 85ºC	
Humidity	**Operating**	0% to 95% (Non-condensing)
	Non-Operating	0% to 95% (Non-condensing)

Reliability		
Data Reliability	Support BCH ECC 66 bit per 1K byte	
Connector Durability	10,000 times	
MTBF	1,000,000 hours	
Endurance (Terabytes Written)	16G	5.17 TB
	32G	10.34 TB
	64G	20.69 TB
	128G	41.39 TB
	256G	82.77 TB

Regulations	
Compliance	CE, FCC and BSMI

Performance

| Model P/N	Read	Write	Random Read (4KB QD32)	Random Write (4KB QD32)
TS16GCFX600	139.1 MB/s	28.31 MB/s	35.62 MB/s	11.66 MB/s
TS32GCFX600	277.3 MB/s	57.89 MB/s	67.67 MB/s	36.65 MB/s
TS64GCFX600	515.5 MB/s	110.7 MB/s	123.6 MB/s	88.66 MB/s
TS128GCFX600	512.4 MB/s	212.7 MB/s	143.0 MB/s	178.5 MB/s
TS256GCFX600	500.1 MB/s	349.6 MB/s	146.2 MB/s	193.7 MB/s

Note: 25 ℃, tested on Gigabyte GA-Z87-UD3H, 4GB RAM, Windows® 7 x86 with AHCI mode, benchmark utility Crystal DiskMark (version 5.2.1), copied file 4000MB.

Actual Capacity

Model P/N	User Max. LBA	Cylinder	Head	Sector
TS16GCFX600	31,277,232	16,383	16	63
TS32GCFX600	62,533,296	16,383	16	63
TS64GCFX600	125,045,424	16,383	16	63
TS128GCFX600	250,069,680	16,383	16	63
TS256GCFX600	500,118,192	16,383	16	63

Power Requirements		
Input Voltage		3.3V ± 5%
Mode		**Max. (mA)**
TS16GCFX600	**Write**(peak)	160.7
	Read(peak)	165.8
	Idle(peak)	71.4
TS32GCFX600	**Write**(peak)	199
	Read(peak)	215.3
	Idle(peak)	74.1
TS64GCFX600	**Write**(peak)	278.6
	Read(peak)	298.5
	Idle(peak)	74.8
TS128GCFX600	**Write**(peak)	413
	Read(peak)	291
	Idle(peak)	71.3
TS256GCFX600	**Write**(peak)	620.3
	Read(peak)	297.8
	Idle(peak)	70.5

Package Dimensions

Below figure illustrates the Transcend CFX600. All dimensions are in mm.
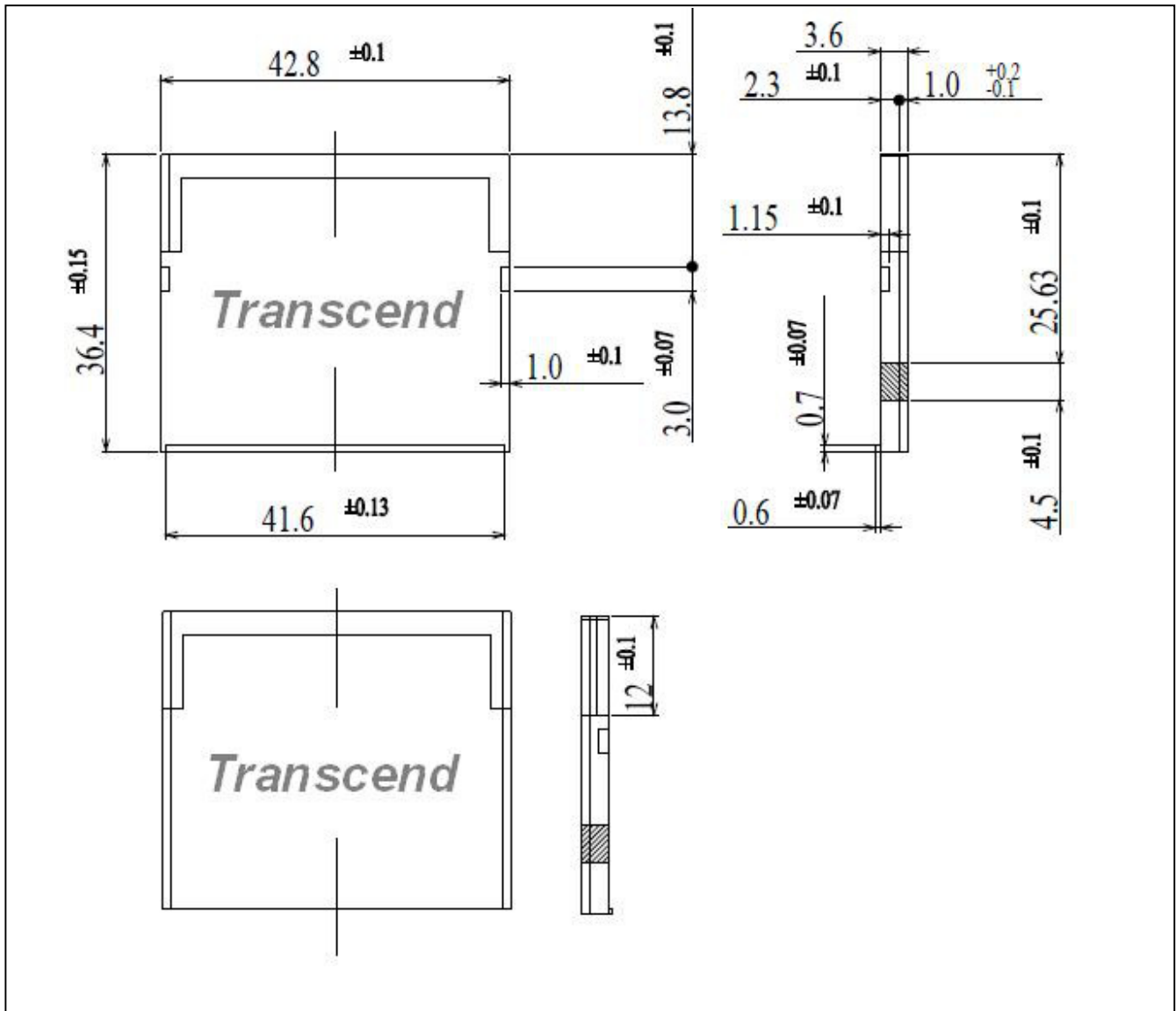
Pin Assignments

Pin No.	Pin Name
7-pin Signal Segment	
S1	GND
S2	A+
S3	A-
S4	GND
S5	B-
S6	B+
S7	GND
17-pin Power Segment	
PC1	CDI
PC2	GND
PC3	DEVSLP
PC4	NC
PC5	NC
PC6	NC
PC7	GND
PC8	NC
PC9	NC
PC10	NC
PC11	NC
PC12	GND
PC13	3.3V
PC14	3.3V
PC15	GND
PC16	GND
PC17	CDO

Pin Layout

Block Diagram

```
┌─────────────────────────────────────────────────┐
│            CFAST™ Interface                      │
└─────────────────────────────────────────────────┘
                      ↕
              ┌───────────────┐
              │  SATA SSD CTL │
              └───────────────┘
                      ↕
        ┌─────────┬─────────┬─────────┐
        ↕         ↕         ↕         ↕
    ┌───────┐ ┌───────┐ ┌───────┐ ┌───────┐
    │ Flash │ │ Flash │ │ Flash │ │ Flash │
    └───────┘ └───────┘ └───────┘ └───────┘
```
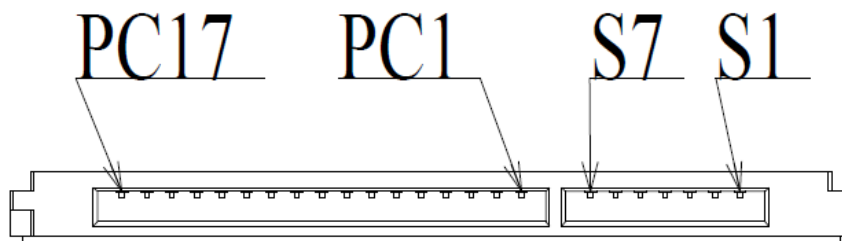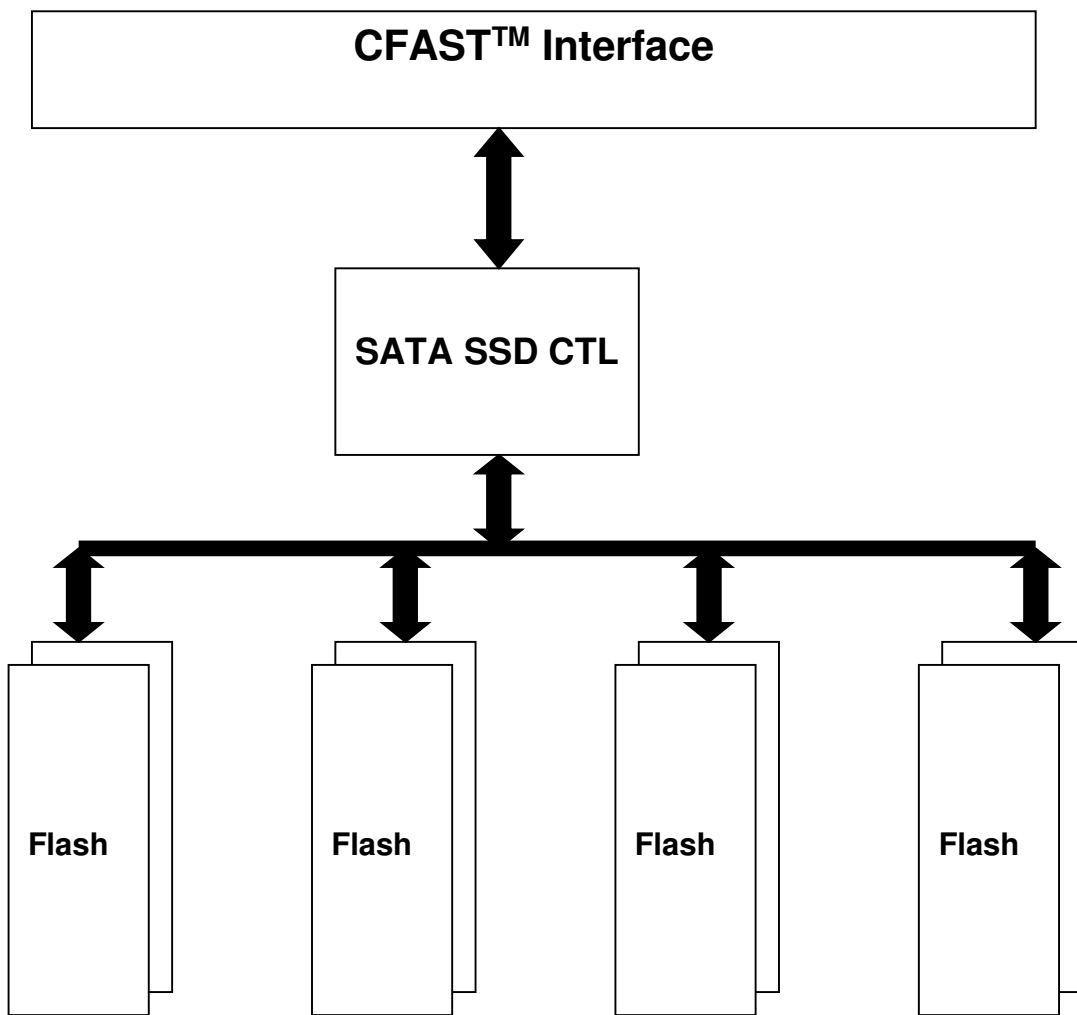
Reliability

Wear-Leveling algorithm

The controller supports static/dynamic wear leveling. When the host writes data, the controller will find and use the block with the lowest erase count among the free blocks. This is known as dynamic wear leveling. When the free blocks' erase count is higher than a threshold value plus data blocks', it will activate the static wear leveling, replacing the less frequently used user blocks with the high erase count free blocks.

ECC algorithm

Using 66 bit BCH Error Correction Code with each channel, the controller can correct 66 random bit per 1K byte data sector for MLC NAND flash. The hardware executes parity generation and error detection/correction features.

Bad-block management

When the flash encounters ECC failed, program fail or erase fail, the controller will mark the block as a bad block to prevent the used of this block and caused data lost later on.

ATA Command Register

This table with the following paragraphs summarize the ATA command set.

Support ATA/ATAPI Command	Code	Protocol
General Feature Set		
EXECUTE DIAGNOSTICS	90h	Device diagnostic
FLUSH CACHE	E7h	Non-data
IDENTIFY DEVICE	ECh	PIO data-In
INITIALIZE DRIVE PARAMETERS	91h	Non-data
READ DMA	C8h	DMA
READ LOG EXT	2Fh	PIO data-In
READ MULTIPLE	C4h	PIO data-In
READ SECTOR(S)	20h	PIO data-In
READ VERIFY SECTOR(S)	40h or 41h	Non-data
SET FEATURES	EFh	Non-data
SET MULTIPLE MODE	C6h	Non-data
WRITE DMA	CAh	DMA
WRITE MULTIPLE	C5h	PIO data-out
WRITE SECTOR(S)	30h	PIO data-out
NOP	00h	Non-data
READ BUFFER	E4h	PIO data-In
WRITE BUFFER	E8h	PIO data-out
Power Management Feature Set		
CHECK POWER MODE	E5h or 98h	Non-data
IDLE	E3h or 97h	Non-data
IDLE IMMEDIATE	E1h or 95h	Non-data
SLEEP	E6h or 99h	Non-data
STANDBY	E2h or 96h	Non-data
STANDBY IMMEDIATE	E0h or 94h	Non-data
Security Mode Feature Set		
SECURITY SET PASSWORD	F1h	PIO data-out
SECURITY UNLOCK	F2h	PIO data-out
SECURITY ERASE PREPARE	F3h	Non-data
SECURITY ERASE UNIT	F4h	PIO data-out
SECURITY FREEZE LOCK	F5h	Non-data
SECURITY DISABLE PASSWORD	F6h	PIO data-out
SMART Feature Set		
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Execute Off-Line Immediate	B0h	Non-data
SMART Read Log	B0h	PIO data-In
SMART Read Data	B0h	PIO data-In
SMART Read Threshold	B0h	PIO data-In
SMART Return Status	B0h	Non-data
SMART Save Attribute Values	B0h	Non-data
SMART Write Log	B0h	PIO data-out
Host Protected Area Feature Set		

Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
48-bit Address Feature Set		
Flush Cache Ext	EAh	Non-data
Read Sector(s) EXt	24h	PIO data-In
Read DMA Ext	25h	DMA
Read Multiple Ext	29h	PIO data-In
Read Native Max Address Ext	27h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write Multiple Ext	39h	PIO data-out
Write Sector(s) Ext	34h	PIO data-out
NCQ Feature Set		
Read FPDMA Queued	60h	DMA Queued
Write FPDMA Queued	61h	DMA Queued
Others		
Data Set Management	06h	DMA
Seek	70h	Non-data

ATA Command Specifications

FLUSH CACHE (E7h)

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

IDENTIFY DEVICE (ECh)

This commands read out 512Bytes of drive parameter information. Parameter Information consists of the arrangement and value as shown in the following table. This command enables the host to receive the Identify Drive Information from the device.

INITIALIZE DEVICE PARAMETERS (91h)

This command enables the host to set the number of logical sectors per track and the number of logical heads minus 1, per logical cylinder for the current CHS translation mode.

READ DMA (C8h)

Read data from sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. A sector count of zero requests 256 sectors.

READ LOG EXT (2Fh)

This 48-bit command is for devices implementing the GPL feature set. It returns the specified log to the host.

READ MULTIPLE (C4h)

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

READ SECTOR(S) (20h)

This command reads 1 to 256 sectors as specified in the Sector Count register from sectors which is set by Sector number register. A sector counts of 0 requests 256 sectors. The transfer beings specified in the Sector Number register.

READ VERIFY SECTOR(S) (40h/41h)

This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

SET FEATURES (EFh)

This command set parameter to Features register and set drive's operation. For transfer mode, parameter is set to Sector Count register. This command is used by the host to establish or select certain features.

SET MULTIPLE MODE (C6h)

This command enables the device to perform READ MULTIPLE and WRITE MULTIPLE operations and establishes the block count for these commands.

WRITE DMA (CAh)

Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value.

WRITE MULTIPLE (C5h)

This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

WRITE SECTOR(S) (30h)

Write data to a specified number of sectors (1 to 256, as specified with the Sector Count register) from the specified address. Specify "00h" to write 256 sectors.

NOP (00h)

The device shall respond with command aborted. For devices implementing the Overlapped feature set, subcommand code 00h in the Features register shall abort any outstanding queue. Subcommand codes 01h through FFh in the Features register shall not affect the status of any outstanding queue.

READ BUFFER (E4h)

The READ BUFFER command enables the host to read a 512-byte block of data.

WRITE BUFFER (E8h)

This command enables the host to write the contents of one 512-byte block of data to the device's buffer.

Power Management Feature Set

CHECK POWER MODE (E5h or 98h)
The host can use this command to determine the current power management mode.

IDLE (E3h or 97h)

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power mode is disabled.

IDLE IMMEDIATE (E1h or 95h)
This command causes the device to set BSY, enter the Idle(Read) mode, clear BSY and generate an interrupt.

SLEEP (E6h or 99h)
This command causes the device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

STANDBY (E2h or 96h)
This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

STANDBY IMMEDIATE (E0h or 94h)
This command causes the drive to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" Mode), clear BSY and return the interrupt immediately.

Security Mode Feature Set

SECURITY SET PASSWORD (F1h)
This command sets user password or master password. The host outputs sector data with PIO data-out protocol to indicate the information defined in the following table.

Security Set Password Data Content 1

Word	Content		
0	Control word		
	Bit 0	Identifier	0=set user password 1=set master password
	Bits 1-7	Reserved	
	Bit 8	Master Password Capability	0=High 1=Maximum
	Bits 9-15	Reserved	
1-16	Password (32 bytes)		
17	Master Password Identifier. This word is valid if word 0 bit 0is set to one.		
18-255	Reserved		

SECURITY UNLOCK (F2h)
This command disables LOCKED MODE of the device. This command transfers 512 bytes of data from the host with PIO data-out protocol. The following table defines the content of this information.

Security Unlock Information 2

Word	Content		
0	Control word		
	Bit 0	Identifier	0=compare user password 1=compare master password
	Bits 1-15	Reserved	
1-16	Password (32 bytes)		
17-255	Reserved		

SECURITY DISABLE PASSWORD (F6h)

Disables any previously set user password and cancels the lock. The host transfers 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, in which the drive compares with the saved password. If they match, the drive cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY ERASE PREPARE (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable erasing and unlocking. This command prevents accidental loss of data on the drive.

SECURITY ERASE UNIT (F4h)

The host uses this command to transfer 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, in which the drive compares with the saved password. If they match, the drive deletes user data, disables the user password, and cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY FREEZE LOCK (F5h)

Causes the drive to enter Frozen mode. Once this command has been executed, the following commands to update a lock result in the Aborted Command error:

• SECURITY SET PASSWORD

• SECURITY UNLOCK

• SECURITY DISABLE PASSWORD

• SECURITY ERASE PREPARE

• SECURITY ERASE UNIT

The drive exits from Frozen mode upon a power-off or hard reset. If the SECURITY FREEZE LOCK command is issued when the drive is placed in Frozen mode, the drive executes the command, staying in Frozen mode.

Identify Device Information Default Value

Word Address	Default Value	Total Bytes	Data Field Type Information
0	044Ah	2	General configuration
1	XXXXh	2	Default number of cylinders
2	XXXXh	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0240h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	XXXXh	20	Serial number in ASCII (Right Justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0000h	2	Obsolete
23-26	XXXXh	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	XXXXh	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	XXXXh	2	Reserved
49	2F00h	2	Capabilities
50	4000h	2	Capabilities
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0007h	2	Field Validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word 57 = LSW, Word 58 = MSW)
59	0101h	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0207h	2	Multiword DMA transfer. Supports MDMA Mode 0,1,and 2
64	0003h	2	Advanced PIO modes supported
65	0078h	2	Minimum Multiword DMA transfer cycle time per word. In PC Card modes this value shall be 0h
66	0078h	2	Recommended Multiword DMA transfer cycle time. In PC Card modes this value shall be 0h

Word Address	Default Value	Total Bytes	Data Field Type Information
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control
69	0100h	2	Additional supported
70-74	0000h	10	Reserved
75	001Fh	2	Queue depth
76	070Eh	2	Serial ATA capacities · Supports Serial ATA Gen3 · Supports Serial ATA Gen2 · Supports Serial ATA Gen1 · Supports PHY event counters log · Supports receipt of host initiated power management requests · Supports Native Command Queuing
77	000Xh	2	Serial ATA Additional capabilities
78	014Ch	2	Serial ATA features supported · Supports DMA Setup Auto-Activate optimization · Supports software setting preservation · Device supports initiating power management · Supports Device Sleep
79	0040h	2	Serial ATA features enabled · Software settings preservation enabled
80	03FCh	2	Mijor version number (ACS-2)
81	0000h	2	Minor version number
82	746Bh	2	Command sets supported 0
83	7D09h	2	Command sets supported 1
84	4163h	2	Command sets supported 2
85-87	XXXXh	6	Command set/feature enabled
88	007Fh	2	Ultra DMA Mode Supported and Selected
89	0001h	2	Time required for a Normal Erase mode Security Erase Unit command
90	0001h	2	Time required for an Enhanced Erase mode Security Erase Unit command
91	0000h	2	Current Advanced power management value
92	FFFEh	2	Master password identifier
93-99	0000h	14	Reserved
100-103	XXXXh	8	Maximum user LBA for 48-bit address feature set
104	0000h	2	Reserved
105	0008h	2	Maximum number of 512-byte blocks per Data Set Management command
106-127	XXXXh	44	Reserved
128	0001h	2	Security status
129-159	XXXXh	64	Vendor specific
160	0000h	2	Power requirement description
161	0000h	2	Reserved
162	0000h	2	Key management schemes supported

163	0000h	2	CF Advanced True IDE Timing Mode Capability and Setting
164-168	XXXXh	10	Reserved
169	0001h	2	Data Set Management supported
170-216	XXXXh	94	Reserved
217	0001h	2	Non-rotating media (SSD)
218-221	0000h	8	Reserved
222	107Fh	2	Transport major revision (SATA Rev 3.1)
223-254	XXXXh	64	Reserved
255	XXXXh	2	Integrity word

SMART Command Support

Value	Command	Value	Command
D0h	Read Data	D5h	Read Log
D1h	Read Attribute Threshold	D6h	Write Log
D2h	Enable/Disable Autosave	D8h	Enable SMART Operations
D3h	Save Attribute Values	D9h	Disable SMART Operations
D4h	Execute OFF-Line Immediate	DAh	Return Status

If the reserved size is below a threshold, status can be read from the Cylinder Register using the Return Status command (DAh).

SMART DATA Structure

BYTE	F / V	Description
0-1	X	Revision code
2-361	X	Vendor specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370	F	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375-385	R	Reserved
386-395	F	Firmware Version/Date Code
396-399	F	Reserved
400-406	V	'SMI2246XT'
407-415	X	Vendor specific
416	F	Reserved
417	F	Program/write the strong page only
418-419	V	Number of spare block
420-510	X	Vendor specific
511	V	Data structure checksum

F=the content of the byte is fixed and does not change.

V=the content of the byte is variable and may change depending on the state of the device or the commands executed by the device.

X=the content of the byte is vendor specific and may be fixed or variable.

R=the content of the byte is reserved and shall be zero.

SMART Attributes

The table below shows the vendor specific data in byte 2 to 361 of the 512-byte SMART data.

Attribute ID (hex)	Raw Attribute Value						Attribute Name
01	MSB	00	00	00	00	00	Read Error Rate
05	LSB	MSB	00	00	00	00	Reallocated sectors count
09	LSB	-	-	MSB	00	00	Power-on hours
0C	LSB	-	-	MSB	00	00	Power Cycle Count
A0	LSB	-	-	MSB	00	00	Uncorrectable sectors count when read/write
A1	LSB	MSB	00	00	00	00	Number of valid spare block
A2	LSB	MSB	00	00	00	00	Number of cache data block
A3	LSB	MSB	00	00	00	00	Number of initial invalid block
A4	LSB	-	-	MSB	00	00	Total erase count
A5	LSB	-	-	MSB	00	00	Maximum erase count
A6	LSB	-	-	MSB	00	00	Minimum erase count
A7	LSB	-	-	MSB	00	00	Average erase count
A8	LSB	-	-	MSB	00	00	Maximum erase count of spec
A9	LSB	-	-	MSB	00	00	Remain Life (percentage)
C0	LSB	-	-	MSB	00	00	Power-off retract Count
C2	MSB	00	00	00	00	00	Controlled temperature
C3	LSB	-	-	MSB	00	00	Hardware ECC recovered
C4	LSB	-	-	MSB	00	00	Reallocation event count
C7	LSB	MSB	00	00	00	00	Ultra DMA CRC Error Count
F1	LSB	-	-	MSB	00	00	Total LBA written (each write unit = 32MB)
F2	LSB	-	-	MSB	00	00	Total LBA read (each read unit = 32MB)
F5	LSB	-	-	MSB	00	00	Total write to flash (each write unit = 32MB)

Ordering Information

TS XG CFX 600

Transcend Product

Capacity
16GB to 256GB

CFast Card

CFast 2.0 with MLC
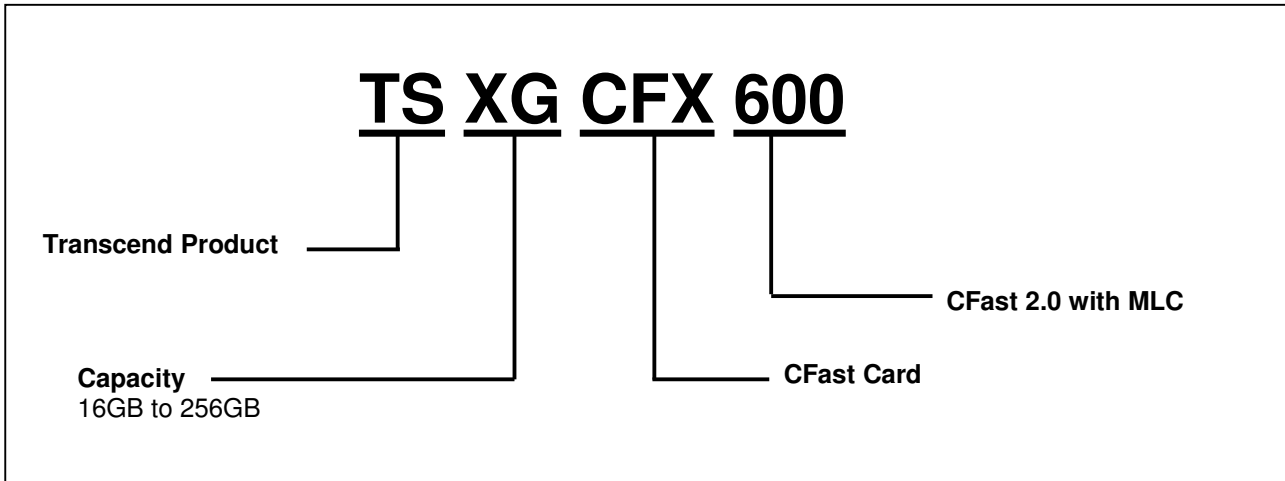
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Transcend®
good memories start here

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Revision History(D)			
Version	**Date**	**Modification Content**	**Modified Page**
V1.0	2017/07/27	Formal release	